of the first inverting logic element and the output impedance.

cont A'

3. (amended) The edge sensitive detection circuit of claim 2, wherein the second inverting logic element comprises an inverter and wherein the first inverting logic element comprises at least one of an inverter and a NAND gate.

A2

10. (amended) The edge sensitive detection circuit of claim 9 further comprises:

Sub B'

a second gating device that provides a second input logic signal to the processing module, wherein the processing module produces a second prccessed logic signal based on the second input logic signal;

a second filter module operably coupled to receive the second processed logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second processed logic signal; and

a second soft latch module cperably coupled to receive the second pulse signal, wherein the second soft latch module latches a logic value in accordance with the second pulse signal.

A3

Sub B'

12. (amended) The edge sensitive detection circuit of claim 9, wherein the soft latch mcdule comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.

18. (amended) The edge sensitive detection circuit of claim 17, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.